IMPACT OF THREADING DISLOCATIONS ON BOTH n/p AND p/n SINGLE JUNCTION GaAs CELLS GROWN ON Ge/SiGe/Si SUBSTRATES

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ABSTRACT

Single junction GaAs solar cells having an n/p polarity were grown on p-type Ge/SiGe/Si substrates for the first time. The cell performance and material properties of these n/p cells were compared with p/n cells grown on n-type Ge/SiGe/Si substrates for which record high minority carrier hole lifetimes of 10 ns and open circuit voltages (V_{oc}) greater than 980 mV (AM0) were achieved[1,2]. The initial n/p experimental results and correlations with theoretical predictions have indicated that for comparable threading dislocation densities (TDD), n/p cells have longer minority carrier diffusion lengths, but reduced minority carrier lifetimes for electrons in the p-type GaAs base layers. This suggests that a lower TDD tolerance exists for n/p cells compared to p/n cells, which has implications for the optimization of n/p high efficiency cell designs using alternative substrates.

INTRODUCTION

The development of high efficiency III-V compound solar cells grown on Si substrates has received sustained interest in the photovoltaics community for more than two decades[1-4]. III-V/Si solar cells are attractive because they combine optimum photovoltaic materials such as InGaP, GaAs, and AlGaAs with an optimum substrate material, Si. Compared to Ge, which is currently the dominant substrate for III-V space photovoltaics, Si possesses far superior substrate properties with respect to mass density, mechanical strength, thermal conductivity, cost, wafer size and availability. Unfortunately, the 4% mismatch in lattice constant between Si and GaAs can generate a high density of threading dislocations in III-V overlayers grown on Si, which can severely reduce GaAs material quality, minority carrier lifetimes, and ultimately solar cell performance.

Nevertheless, many groups have recognized the potential benefits of epitaxial III-V/Si solar cells, and III-V/Si integration in general, thus leading to investigations of methods to control and reduce threading dislocation densities in this highly mismatched heterostructure. These groups have been successful in reducing threading dislocation densities in the III-V overlayers from ~ 10^9-10^{10} cm^{-2} for direct GaAs on Si epitaxy to ~$2x10^6$-$1x10^7$ cm^{-2} range[4-9]. In these works, the minority carrier lifetimes in GaAs are 1-4 ns and open circuit voltages for p/n single junction GaAs cells are typically on the order of 900 mV or lower under AM0 conditions[8,9]. The TDD reduction methods referenced above all utilize III-V materials to obtain the GaAs lattice parameter; another approach is to accommodate the lattice mismatch prior to any III-V epitaxy. By growth of step-graded $Si_{1-x}Ge_x$ layers, up to 100% Ge, on Si substrates the lattice mismatch is addressed in a non-polar material system and under growth conditions that are independent from the III-V solar cell growth conditions. This "virtual Ge substrate" approach has resulted in threading dislocations as low as $8x10^5$ cm^{-2} within relaxed GaAs overlayers[10,11]. A representative TEM image for a GaAs overlayer on a SiGe substrate grown by solid source molecular beam epitaxy (SSMBE) is shown in Fig. 1.

The impact of this lower threading dislocation density and a controlled GaAs/Ge interface has yielded the highest minority carrier lifetimes reported to date for GaAs grown on Si, with values in excess of 10 ns being demonstrated in n-type GaAs[9,10]. A record high AM0 open circuit voltages for verified single junction cells, greater than 980 mV, has also been achieved[1,2]. In this paper, we report the first results for single junction n/p GaAs cells on p-type SiGe substrates. Since III-V n/p cells are attractive due to their superior radiation hardness, it is important to investigate the affect of TDDs on cell performance for this cell configuration. Although these cells were grown on substrates with a higher TDD due to the present state of p-type substrate development, the n/p cell performance characteristics were compared to previous p/n results to begin investigating the possible differences in design constraints for the different polarity cells.

EXPERIMENTAL

Step graded SiGe buffers were grown by chemical vapor deposition on (001) Si wafers with a 6° off-cut toward the [110] direction. The grading procedures for n-type SiGe substrates, as previously reported, provide a virtual Ge

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substrate with a TDD of 8-10x10^5 cm^{-2} [12] for p/n cells. The process includes a high temperature grade coupled with a chemical mechanical polish (CMP) process to unlock pinned dislocations, which is an essential step for ultimately achieving lower TDD values[12]. To investigate the performance of n/p configuration cells, the first p-type virtual Ge substrates were grown. A Ge doping concentration of approximately 1x10^{19} cm^{-3} was utilized. At this early stage in process development of 8-inch SiGe substrates for this work, the CMP process was not used, thus resulting in a higher TDD value of ~4x10^6 cm^{-2}, as measured by etch pit density measurements. The higher TDD of p-type substrates limits the efficiency of the n/p cell;

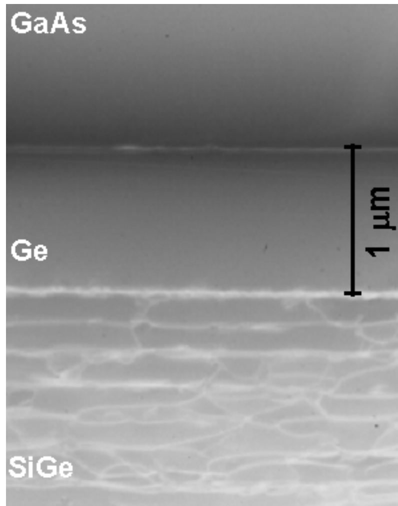

Fig. 1: A X TEM micrograph of a GaAs layer grown on a Ge/SiGe/Si substrate (TDD ~ 1x10^6 cm^{-2}).

however, it provides a basis for the first experimental comparison for n/p and p/n cells on Si-based substrates.

In all cases, the growth initiation procedure for GaAs on Ge/SiGe/Si was completed by SSMBE as described in Ref. 13. The p/n configuration GaAs single junction cells were grown via low pressure metal organic vapor deposition (MOCVD) at 620°C; $In_{0.5}Ga_{0.5}P$ window layers and back surface fields were used. The p/n cell had an emitter thickness of 0.4 μm and a base thickness of 2.0 μm. The n/p configuration single junction GaAs cells utilized $In_{0.5}Ga_{0.5}P$ window layers and $Al_{0.2}Ga_{0.8}As$ back surface fields. These cells were grown via SSMBE at substrate temperatures of 490°C/600°C/620°C for the $In_{0.5}Ga_{0.5}P$/GaAs/$Al_{0.3}Ga_{0.7}As$ layers, respectively. The n/p cell utilized a 0.05 μm emitter thickness and a 3.0 μm base thickness. In both the n/p and p/n cells, the base doping values were ~2x10^{17} cm^{-3} and the emitter doping values were ~4x10^{18} cm^{-3}. The cells were electrically isolated by mesa-etching and the contact layers were removed with selective-etching just prior to the antireflection coating (ARC) deposition. Front contact was made to a highly doped GaAs contact layer, Au/Cr was used for contact to p-type GaAs and Ni/Ge/Au was used for contact to n-type GaAs; Al was used for both p-type and n-type back contacts to silicon. The anti-reflection coating deposited was 75Å MgF_2 / 480Å ZnS / 990Å MgF_2. The cells discussed here range in size from 0.044 cm^2 to 0.36 cm^2 with metal coverage from 10% to 8%, respectively. Solar cell structures were evaluated by dark J-V, light J-V under AM0 illumination, spectral response measurements.

RESULTS AND DISCUSSION

Impact of TDD on minority carrier properties

The impact of TDD on minority carrier properties in n-type material has been well documented[3,14]. Previous work has shown a 10 ns hole lifetime in n-type (n~2x10^{17} cm^{-3}) GaAs on SiGe (TDD~1x10^6 cm^{-2}) as measured by time-resolved photoluminescence; this lifetime corresponds to a minority carrier diffusion length for holes (L_p) of 2.7 μm (given D_p=7.1 cm^2/s) which allows collection of minority carriers throughout the 2.0 μm base thickness of a p/n cell. This diffusion length was substantiated for p/n cells since consistent external quantum efficiencies for solar cells grown on GaAs, Ge, and SiGe substrates have been shown[1,2]. However, when p-type SiGe substrates are used with a TDD of ~4x10^6 cm^{-2}, the theoretical minority carrier diffusion length for electrons (L_n) in p-type GaAs indicates that collection in the base of an n/p cell should be limited. The deficiency in the external quantum efficiency in the long wavelengths for the n/p cell grown on SiGe compared to cells grown on GaAs and Ge, as seen in Fig. 2, clearly indicates that L_n is less than the 3 μm base thickness. Estimating L_n from the spectral response data using an analytical model, a minority carrier diffusion length of ~1.8 μm in the p-type base is predicted [15].

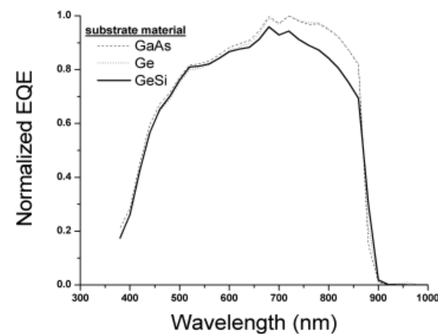

Fig. 2: A comparison of the normalized external quantum efficiency for n/p single junction GaAs solar cells grown on p-type GaAs, Ge, and SiGe substrates. The SiGe substrate had a TDD of ~4x10^6 cm^{-2}.

Using the NTT model[14] and a maximum minority carrier diffusion length for electrons in p-type GaAs (p~2x10^{17} cm^{-3}) and holes in n-type GaAs (n ~ 2x10^{17} cm^{-3}) of 19.7 μm and 4.2 μm, respectively [16], the minority carrier diffusion length as a function of TDD was calculated and is shown in Fig. 3a. The experimental values obtained in this study for the n-type base (p/n cell) and the p-type base (n/p cell) have been plotted and there is good agreement with this model. Unlike the case for a TDD of ~4x10^6 cm^{-2}, the electron minority carrier diffusion length for a p-type base

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with a TDD of ~1x10^6 cm^{-2} results in a value of 3.5 μm, which would not limit carrier collection in the base of an n/p cell. However, while this longer diffusion length will maintain a high short circuit current density, J_{sc}, due to efficient collection in the cell's base, this will not necessarily translate to optimum cell efficiency unless high minority carrier lifetimes for electrons are also obtained. Fig. 3b shows the minority carrier lifetime as a function of TDD; these values were calculated using Eq. 1 and by assuming a maximum lifetimes components, τ_n =50 ns and τ_p =25 ns, and minority carrier diffusion coefficients, D_n=78 cm^2/s and D_p=7.1 cm^2/s[16].

$$\frac{1}{\tau} = \frac{1}{\tau_{\max}} + \frac{\pi^3 D[TDD]}{4} \qquad (1)$$

For a TDD of ~1x10^6 cm^{-2}, the calculated electron lifetime is 1.6 ns, this is significantly lower than that measured and calculated for holes of 10 ns. This lower lifetime translates to a higher depletion region recombination current and thus a lower open circuit voltage for cells whose V_{oc} is largely limited by depletion region recombination. From this equation and figure, it is clear that minority carrier diffusion

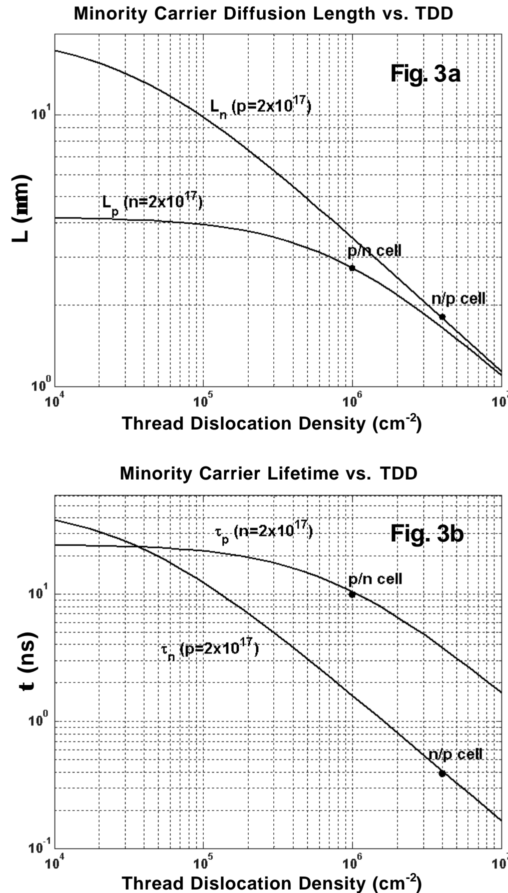


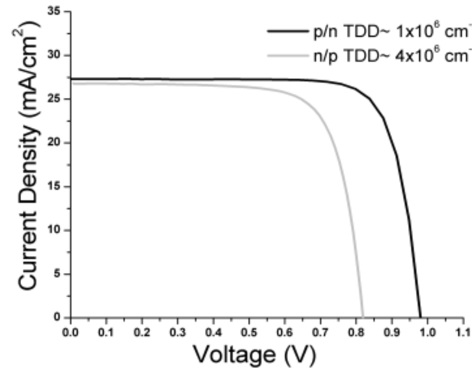
Fig. 3: Theoretical plot of minority carrier diffusion length (Fig. 3a) and minority carrier lifetime (Fig. 3b) for both n-type and p-type GaAs with a doping concentrations of 2x10^{17} cm^{-3}. Experimentally extracted values for GaAs grown on SiGe substrates are included in the plots.

coefficients and thus the minority carrier mobilities in solar cell materials are important design parameters when accommodating dislocated substrates.

Impact of TDD on open-circuit voltage

The results for the p/n cells on SiGe substrates have shown record high open circuit voltages (V_{oc}) greater than 980 mV. In some cases, active Ge interfaces have increase V_{oc} beyond 1000 mV[2]. In this discussion, we will limit the results to verified single junction devices where Ge inactivity has been confirmed by photo-voltage measurements. Fig. 4 compares the light J-V characteristic under AM0 illumination for the p/n and n/p cells on SiGe described earlier. The device performance characteristics are also given in Fig. 4.

To correlate these experimental results with minority carrier properties discussed earlier, the open circuit voltage, V_{oc}, was calculated as a function of TDD based on Eq. 2 and Eq. 3 and by using an intrinsic carrier concentration, n_i, of 2.6x10^5 cm^{-3}, a depletion width, W, using on base and emitter doping values and the abrupt junction approximation, and τ values from Fig. 3.



	p/n	n/p
V_{oc} (mV)	980	819
FF (%)	78.3	74.1
J_{sc} (mA/cm^2)	27.8	27.3
η (%)	15.6	12.0
A (cm^2)	0.044	0.36
metal (%)	10	8
TDD (cm^{-2})	1x10^6	4x10^6

Fig. 4: Light J-V response under AM0 conditions for representative single junction p/n and n/p cells grown on SiGe substrates with the corresponding device performance characteristics (courtesy of NASA Glenn Research Center).

Since dark J-V analysis indicated an ideality factor of n=2 for both n/p and p/n diodes, the depletion region recombination current, J_{or}, was used in place of the reverse saturation current density, J_o, in Eq. 3.

$$J_{or} = 0.5 q n_i W \tau \qquad V_{oc} = \left(\frac{nkT}{q}\right)\ln\left(\frac{J_{sc}}{J_o} + 1\right) \qquad (2,3)$$

Moreover, a constant value of J_{sc} that is typical for high efficiency single junction GaAs cells under AM0 illumination (32 mA/cm^2) was used; therefore, this plot represents an

overestimate of V_{oc} because the J_{sc} will be over estimated at higher TDD values where minority carrier diffusion lengths can limit collection (see Fig. 2). The experimental results from Fig. 4 are included in Fig. 5. There are at least two implications from this figure. First, as has been shown in earlier work for p/n cells on n-type SiGe substrates, the fact that the measured V_{oc} and diffusion length values lie on or above the theoretical dependence on TDD shows that all other performance limiting defects, such as anti-phase domains, point defect, inter-diffusion, etc. have been eliminated or suppressed to negligible levels for n/p cells on p-type SiGe substrates. Secondly, under the assumption of this simple model, n/p configured cells appear more sensitive to TDD than p/n, meaning that careful design approaches for n/p cells must be implemented to mitigate the impact of TDD in the range of $0.5 - 1\times10^{6}$ cm^{-2}. This work is currently underway.

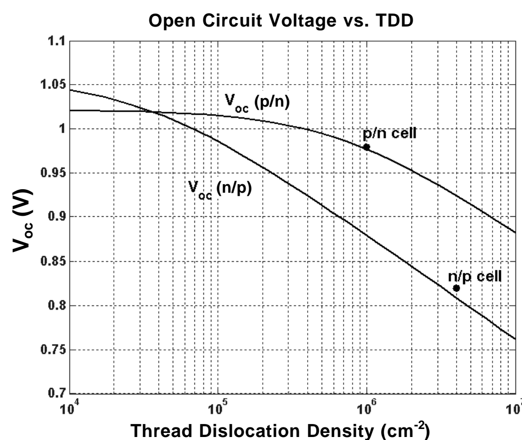


Fig. 5: Theoretical plot of V_{oc} as a function of TDD, assuming that depletion region recombination dominates the reverse saturation current density and a constant light current, J_{sc} = 32 mA/cm^2; thus V_{oc} is overestimated.

CONCLUSIONS

Single junction GaAs solar cells having an n/p polarity were grown on p-type Ge/SiGe/Si substrates for the first time. The cell performance and material properties of these n/p cells were compared with p/n cells grown on n-type Ge/SiGe/Si substrates. Given that the mobility for electrons in GaAs is fundamentally higher than that for holes, depletion region recombination is enhanced in p-type material where threading dislocations are present. This suggests that a lower TDD tolerance exists for n/p cells compared to p/n cells without accounting for cell design optimization.

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REFERENCES

[1] J.A. Carlin, M.K. Hudait, S.A. Ringel, D.M. Wilt, E.B. Clark, C.W. Leitz, M .Currie, T .Langdo, E.A. Fitgerald. *28 th IEEE Photovoltaic Specialists Conference*, Alaska, September 2000; 1006-1011.

[2] S.A. Ringel, J.A. Carlin, C.A. Andre, D.M. Wilt, E.B. Clark, C.W. Leitz, E.A. Fitgerald, A.A. Allerman, submitted to *Progress in Photovoltaics* 2002.

[3] J.C.C. Fan, C.O. Bozler, R.W. McClelland. *15th IEEE Photovoltaic Specialists Conference*, Kissimmee, FL, May 1981; 666-672.

[4] M. Yamaguchi. *Journal of Materials Research* 1991; **6** (2): 376-384.

[5] R.K. Ahrenkiel, M.M. Al-Jassim, B. Keyes, D. Dunlavy, K.M. Jones, S.M. Vernon, T.M. Dixon. *Journal of Electrochemical Society* 1990; **137** (3): 996-1000.

[6] R. Venkatasubramanian, M.L. Timmons, J.B. Posthill, B.M. Keyes, R.K. Ahrenkiel. *Journal of Crystal Growth* 1991; **107** (1-4): 489-493.

[7] A. Freundlich, M. Lerouz, J.C. Grenet, A. Leycuras, G. Neu, C. Verie. *Proceedings of the 8th European Photovoltaic Specialists Conference*, Florence, Italy, May 1988; 1522-1526.

[8] G. Wang, K.Ohtsuka, M. Kawai, T. Soga, T. Jimbo, M. Umeno. *Proceedings of 2nd World Conference On Photovoltaic Solar Energy Conversion*, Vienna, Austria, July 1998; 3733-3736.

[9] G. Wang, G.Y. Zhao, T. Soga, T. Jimbo, M. Umeno *Japanese Journal of Applied Physics Part* 2 1998; **37** (11A): L1280-L1282.

[10] R.M. Sieg, J.A. Carlin, J.J. Boeckl, S.A. Ringel, M.T. Currie, S.M. Ting, T.A. Langdo, G. Taraschi, E.A. Fitzgerald, B.M. Keyes. *Applied Physics Letters* 1998; **73** (21): 3111-3113.

[11] J.A. Carlin, S.A. Ringel, E.A. Fitzgerald, M. Bulsara, Keyes BM. *Applied Physics Letter* 2000; **76** (14): 1884-1886.

[12] M.T. Currie, S.B. Samavedam, T.A. Langdo, T.A. Leitz, E.A. Fitzgerald. *Applied Physics Letter* 1998; **72** (14): 1718-1720.

[13] R.M Sieg, S.A. Ringel, S.A. Ting, E.A. Fitzgerald, R. Sacks. *Journal of Electronics Materials* 1998; **27** (7): 900-907.

[14] M. Yamaguchi, C. Amano. *Journal of Applied Physics* 1985; **58** (9): 3601-3606.

[15] Y. Hamakawa and Y. Kuwano, *Solar Energy Engineering*, Advanced Electronics series Vol. 3 (Baifukan, Toyota, 1995), 22.

[16] M.R. Brozel and G.E. Stillman, *Properties of Gallium Arsenide, Data Review Series No. 16*, Ch. 2 (INSPEC, London, 1996), 39-88.